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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,998	05/04/2001	James S. Chapple	42390.P9943	8977

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EXAMINER
PATEL, NIKETA I

ART UNIT	PAPER NUMBER
2182	

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DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/848,998	CHAPPLE ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirairi U.S. Patent Number: 6,480,942 (hereinafter referred to as "*Hirairi*") and further in view of 'Data Structures with C++' by William Ford & William Topp (hereinafter referred to as "*Ford & Topp*".)

3. **Referring to claims 1 and 20,** *Hirairi* teaches an apparatus and a method comprising: a queue [see column 5 - lines 34-42]; an event selection logic unit [see figure 6 - element 11] to receive a queue enter signal [see figure 6 - element "WRITE ENABLE"], a queue exit signal [see figure 6 - element "READ ENABLE"], and a queue not empty signal from the queue [see figure 6 - elements 11, 16, 15]; and a counter to increment in response to an increment event signal delivered by the event selection logic unit, the counter to decrement in response to a

decrement event signal delivered by the event selection logic unit [see figure 6 - element 14; column 9 - lines 63-67; column 10 - 1-28] however *Hirairi* fails to explicitly set forth the limitation of the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well know in the computer art to get the advantage of being able to manage a queue by asserting queue enter, exit, empty and full signals in response to a queue event [see *Ford & Topp* pages 204-208] It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to assert queue enter, exit, empty and full signals in response to a queue event to get this advantage.

4. **Referring to claim 2**, *Hirairi* teaches that the event selection logic unit to further receive an inverted version of the queue not empty signal [see figure 6 - elements 11, 16, 15.]

5. **Referring to claim 3**, *Hirairi* teaches further comprising a data register coupled to the counter [see figure 6 - elements

"CONSTANT: MAXIMUM NUMBER OF FIFO ENTRIES", "CONSTANT: 0"; column 10 - lines 55-67; column 11 - lines 1-8.]

6. **Referring to claims 4 and 22**, *Hirairi* teaches an apparatus and a method further comprising a comparator [see figure 7A - element 14; figure 7B - elements 1B, 1A] including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the counter, and the output provided to the event selection logic unit [see figure 7A - element 14; figure 7B - elements 1B, 1A; column 11 - lines 12-38.]

7. **Referring to claim 5**, *Hirairi* teaches that the event selection logic including programmable function to allow a variety of combinations of the queue enter, queue exit, queue not empty, and comparator output signals to serve as increment or decrement events [see figure 6 - elements 1, 11, 16, 15; column 9 - lines 63-67; column 10 - lines 1-28.]

8. **Referring to claim 6**, *Hirairi* teaches further comprising a block of registers including a command register and a status register [see figure 6 - elements 12, 13, 14, 16, 15, 18, 17.]

9. **Referring to claim 21**, *Hirairi* teaches further comprising storing the counter value in a data register [see figure 6 - elements 14, 16, 15; column 9 - lines 63-67; column 10 - lines 1-67; column 11 - lines 1-55.]

10. **Referring to claims 7 and 12,** *Hirairi* teaches a queue [see column 5 - lines 34-42], an event selection logic unit [see figure 6 - element 11] to receive a queue enter signal [see figure 6 - element "WRITE ENABLE"], a queue exit signal [see figure 6 - element "READ ENABLE"], and a queue not empty signal from the queue [see figure 6 - elements 11, 16, 15]; and a first counter to increment in response to a first increment event signal delivered by the event selection logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event selection logic unit [see figure 6 - element 14; column 9 - lines 63-67; column 10 - 1-28.] *Hirairi* fails to explicitly set forth the limitation of a second counter to increment in response to a second increment event signal delivered by the event selection logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event selection logic unit and the second counter to increment in response to the comparator output indication that the first counter value matches the data register value.

One of ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the FIFO control system of *Hirairi* to have a second counter to increment in response to a increment signal

and decrement in response to decrement signal to allow for a second FIFO read and write functions to be recorded. It is for this reason that one of ordinary skill in the art would have been motivated to implement a second counter to a increment signal and decrement in response to decrement signal to allow a FIFO entry and exit functions to be recorded.

Hirairi fails to explicitly set forth the limitation of the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well know in the computer art to get the advantage of being able to manage a queue by asserting queue enter, exit, empty and full signals in response to a queue event [see *Ford & Topp* pages 204-208] It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to assert queue enter, exit, empty and full signals in response to a queue event to get this advantage.

11. **Referring to claim 8**, *Hirairi* teaches that the event selection logic unit to further receive an inverted version of the queue not empty signal [see figure 6 - elements 11, 16, 15.]

12. **Referring to claim 9**, *Hirairi* teaches further comprising a data register coupled to the first counter [see figure 6 - elements "CONSTANT: MAXIMUM NUMBER OF FIFO ENTRIES", "CONSTANT: 0"; column 10 - lines 55-67; column 11 - lines 1-8.]

13. **Referring to claim 10**, *Hirairi* teaches further comprising a comparator [see figure 7A - element 14; figure 7B - elements 1B, 1A] including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the first counter, and the output provided to the event selection logic unit [see figure 7A - element 14; figure 7B - elements 1B, 1A; column 11 - lines 12-38.]

14. **Referring to claim 11**, *Hirairi* teaches the event selection logic including programmable functions to allow a variety of combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events [see figure 6 - elements 1, 11, 16, 15; column 9 - lines 63-67; column 10 - lines 1-28.]

15. **Referring to claim 13**, *Hirairi* teaches further comprising a block of registers including a command register and a status register [see figure 6 - elements 12, 13, 14, 16, 15, 18, 17.]

16. **Referring to claim 14**, *Hirairi* teaches a queue [see column 5 - lines 34-42]; an event selection logic unit [see figure 6 - element 11] to receive a queue enter signal [see figure 6 -

element "WRITE ENABLE"], a queue exit signal [see figure 6 - element "READ ENABLE"], and a queue not empty signal from the queue [see figure 6 - elements 11, 16, 15]; and a counter to increment in response to an increment event signal delivered by the event selection logic unit, the counter to decrement in response to a decrement event signal delivered by the event selection logic unit [see figure 6 - element 14; column 9 - lines 63-67; column 10 - 1-28.] *Hirairi* fails to explicitly set forth the limitation of system with a processor.

17. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that a processor was old and well known in the computer art to be used with FIFO system to allow the data in the FIFO system to be processed. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to implement *Hirair's* invention to include a processor to process data within the FIFO system.

Hirairi fails to explicitly set forth the limitation of the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry.

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention that it was old and well know in the computer art to get the advantage of being able to manage a queue by asserting queue enter, exit, empty and full signals in response to a queue event [see *Ford & Topp* pages 204-208] It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to assert queue enter, exit, empty and full signals in response to a queue event to get this advantage.

18. **Referring to claim 15**, *Hirairi* teaches that the event selection logic unit to further receive an inverted version of the queue not empty signal [see figure 6 - elements 11, 16, 15.]

19. **Referring to claim 16**, *Hirairi* teaches further comprising a data register coupled to the counter [see figure 6 - elements "CONSTANT: MAXIMUM NUMBER OF FIFO ENTRIES", "CONSTANT: 0"; column 10 - lines 55-67; column 11 - lines 1-8.]

20. **Referring to claim 17**, *Hirairi* teaches further comprising a comparator [see figure 7A - element 14; figure 7B - elements 1B, 1A] including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the counter, and the output provided to the event selection logic unit [see figure 7A - element 14; figure 7B - elements 1B, 1A; column 11 - lines 12-38.]

21. **Referring to claim 18**, *Hirairi* teaches that the event selection logic including programmable function to allow a variety of combinations of the queue enter, queue exit, queue not empty, and comparator output signals to serve as increment or decrement events [see figure 6 - elements 1, 11, 16, 15; column 9 - lines 63-67; column 10 - lines 1-28.]

22. **Referring to claim 19**, *Hirairi* teaches further comprising a block of registers including a command register and a status register [see figure 6 - elements 12, 13, 14, 16, 15, 18, 17.]

Response to Arguments

23. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following documents have been made record of to further show the state of the art as it pertains to gathering queue performance data:

Ishida U.S. Patent Number: 6,556,572

Saitoh U.S. Patent Number: 5,805,883

Krakirian U.S. Patent Number: 5,450,546

Dennin et al. U.S. Patent Number: 6,401,149

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (703) 305 4893. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308 3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

The above listed phone numbers of the examiner Niketa I. Patel and the examiner's supervisor, Jeffrey A. Gaffin are effective until October 12, 2004. After October 12, 2004 Niketa I. Patel can be reached at (571) 272-4156 and Jeffrey A. Gaffin can be reached at (571) 272-4146.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP
09/29/2004

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